RF ELECTRONICS DIGITAL CHIRP FOR THE SPACEBORNE IMAGING RADAR-C INSTRUMENT

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Abstract- The SIR-C RF electronics subsystem generates the multifrequency RF signals to drive the antenna distributed array high power amplifiers. The digital frequency step chirp signals are designed to allow flexibility in the selection of radar parameters such as range bandwidth to improve resolution, and pulsewidth to reduce dc power usage.

I. INTRODUCTION

SIR-C is the next critical step in the series of Shuttle radar experiments that began with SIR-A [1] in 1981 and SIR-B [2] in 1984. The SIR-C instrument is designed to demonstrate innovative engineering techniques such as digital frequency step chirp generation to allow multiparameter selection [3,4]. The previously flown experiments in the Spaceborne Imaging Radar series used passive dispersive delay lines to generate the chirp signals instead of the active device for SIR-C.

II. SIR-A/B ANALOG CHIRP

The Shuttle Imaging Radars-A/B (SIR-A/B) utilized passive dispersive delay lines (DDLs) to generate linear frequency modulated (LFM), or chirp, signals. An impulse of three cycles of the Stable Local Oscillator (STALO) was input to the Surface Acoustic Wave (SAW) DDL device, and the chirp output response was amplified and filtered. The SIR-A/B output pulse duration was 33.4 microsec; the SIR-A/B RF bandwidths were 6 and 12 MHz, for chirp slopes of 0.359 and 0.179 MHz/microsec, respectively. Since SIR-A had a different chirp slope than SIR-B, a separate DDL device was required.

The SIR-A/B RF pulse generation process is shown in Figure 1a. The chirp pulse from the DDL device is offset as a lower sideband of STALO. This chirp signal undergoes a dual conversion, being mixed first with 3 x STALO and last with 18 x STALO. The filtered RF output is offset from 14 x STALO.

The advantage of using the passive DDL devices is that they are very stable de-

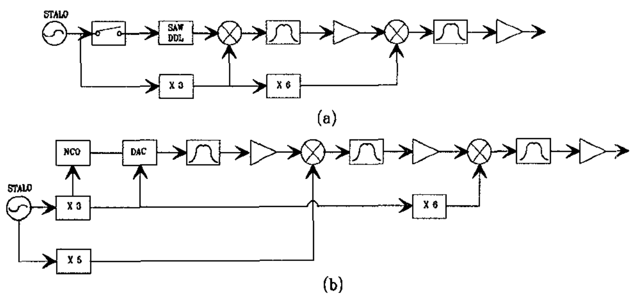

Figure 1. RF Pulse Generation Schemes (a) SIR-A/B, (b) SIR-C

vices, with fixed, well-known characteristics. The disadvantages of the DDLs are the high costs and long lead times.

III. SIR-C DIGITAL CHIRP DESIGN

The SIR-C RF electronics subsystem (RFES) chirp generator subassembly provides the multifrequency RF signals to drive the antenna distributed array high power amplifiers and generates calibration tones to inject into the antenna, thereby providing built-in-test capability. The crucial timing signal, from which the entire instrument derives its RF signals and timing, is produced via a stable local oscillator (STALO) within the RFES, and the interface circuitry is contained within the chirp generator subassembly.

The digital chirp generator successively steps a CW tone across the bandwidth BW over the pulse duration PW to approximate a linear FM chirp signal. This allows flexibility in the selection of the radar parameters of range bandwidth to improve resolution, and pulsewidth to reduce dc power usage. This frequency-step chirp is defined by several key parameters: the start frequency, f_0; frequency step size; step duration; and number of steps, n. The step duration is 40/STALO for the 10 MHz bandwidth and 33.8 microsec pulsewidth case, and 20/STALO for all other cases. The frequency step size is k x 131.8275 KHz, where k=1,2, or 4. The start frequency is set by a number in a PROM. Analysis has shown that the number of frequency steps must be greater than the square root of the time-bandwidth product in order to maintain a low integrated sidelobe ratio for the compressed signal. Test results of the flight chirp generator indicate that it fulfills all specifications.

The SIR-C digital chirp generator uses a numerically controlled oscillator. The step frequency generation scheme is shown in Figure 2. Two clocks are required: STALO/20 and 3 x STALO. The change of phase at each clock cycle is accumulated by adding to the previous value of phase. The phase values are passed to a look-up table and a resulting digital sine waveform with very precise frequency is generated. The 8 most significant bits (MSBs) from the table are passed to a digital-to-analog converter, and the resulting signal is bandpass filtered.

The SIR-C RF pulse generation process is shown in Figure 1b. The step frequency pulse is offset as a lower sideband of STALO. This chirp signal undergoes a dual conversion, being mixed first with 5 x STALO and last with 18 x STALO. The filtered RF output is offset from 14 x STALO.

The advantage of using the active NCO/DAC devices is that they are also very stable devices, with great flexibility. The disadvantages of the active devices are the added power requirements and slightly higher risk of electronic failure. However, redundant units are provided for SIR-C to reduce the risk.

IV. SIR-C DIGITAL CHIRP HARDWARE

The SIR-C RF electronics assembly consists of 28 subassemblies, all of which are positioned upon a baseplate; heat is dissipated from the subassemblies to the baseplate and onto the pallet actively-cooled coldplate. There are two chirp generator subassemblies for redundancy. The Shuttle has only moderate constraints on power and weight, such that the 30 watts of dc power and 4.5 kilograms of mass for each of the RFES chirp generator subassemblies pose no problem. The L-shaped modules are contained within a 11 inch by 9.2 inch by 1.75 inch envelope. Modularity provides ease of testing and assembly and avoids layer building. Power supplies are provided in each subassembly, providing redundancy and ease of testing. The redundant subassembly assures that no one failure will eliminate both L- and C-band radars.

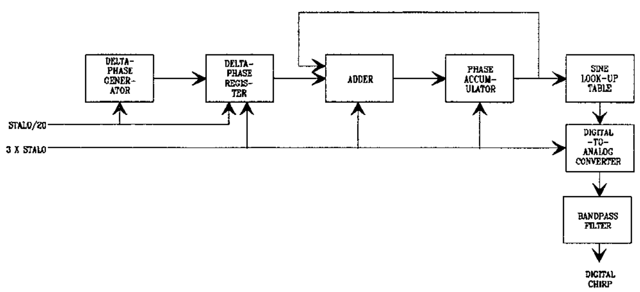

Figure 2. SIR-C Step Frequency Chirp Generator

Four printed circuit boards are contained in the RFES chirp generator subassembly. The heat dissipated by the devices on the boards is routed to the chassis and on to the baseplate and coldplate. The key components on the boards, besides the TTL and ECL logic ICs, are the NCO and the DAC. The NCO, which dissipates 7 watts, is mounted on a 1.5 inch by 1.5 inch pad and uses integral heat sink mounting studs. The DAC is an 0.6 inch by 1.2 inch ceramic dual in-line package (DIP), mounted to the board.

V. SUMMARY

The previously flown SIR-A/B experiments used passive dispersive delay lines to generate the chirp signals. The SIR-C instrument utilizes a digital frequency step chirp generator to allow flexibility in the selection of radar parameters such as range bandwidth to improve resolution, and pulsewidth to reduce dc power usage.

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